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10/606,753	06/27/2003	Robert B. Magill	32172-188433	5555

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EXAMINER	
O CONNOR, BRIAN T	

ART UNIT	PAPER NUMBER
2619	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/606,753	MAGILL ET AL.	
	Examiner	Art Unit	
	BRIAN T. O'CONNOR	2619	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is in response to applicant's amendment filed on 03/27/2008.

2. Claims 1-19 are currently pending.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1-3, 8-9, 12, and 17-19 are rejected under 35 U.S.C. 103(a) as being obvious over Chao et al. (Chao et al., "Delay-Bound Guarantee in Combined Input-Output Buffered Switches", 1 December 2000, IEEE GLOBECOM 2000, Volume 1, pg 515-524; hereafter Chao) cited in IDS dated 10/29/2003 in view of Wu et al. (US 7,177,314; hereafter Wu).

With respect to claim 1, Chao discloses a Combined Input-Output Buffered (CIOB) switch using fixed-sized cells (Abstract, first paragraph, left column, pg 515) containing a multitude of input queues (session queues in IPC1 of Figure 3), a multitude of output queues (session queues in OPC1 of Figure 3); a switch fabric (X01, X11, X0, X1N of Figure 3; Non-blocking switch of Figure 1) that connects the multitude of input queues to the multitude of output queues and must have memory to store and move cells from the input queues to the output queues. Chao's CIOB switch also has an input port controller (IPC1 of Figure 3) and an output port controller (OPC1 of Figure 3) for calculating incoming cell priorities and moving cells from the input queues to the switch

and moving cells from the switch to the output queues (Section V: The Implementation of the SHLS Scheme, right column, pg 519 – third paragraph, left column, pg 521).

Chao does not disclose a controller that determines input priorities for cells from input queues and output priorities for cells from switch fabric to output queues.

Wu, in a invention of scheduling cells across a switch crossbar (Abstract), discloses a controller (12 of Figure 2) that determines input priorities for cells from input queues and output priorities for cells from switch fabric to output queues (column 4, lines 14-26; column 5, lines 13-31).

Wu realizes the benefit of more scalability by using a dedicated controller to move cells/packets across the input queues, switch fabric, and output queues (column 2, lines 55-67). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the controller of Wu with the system of Chao.

With respect to claim 2, Chao further discloses that the fabric orders the transmission of cells to the output queues by virtual finishing time and the cells with the smallest virtual finishing time have the highest priority (Step 3: Accept, left column, pg 517 – first paragraph, right column, pg 517).

With respect to claim 3, Chao further discloses that the IPC1 and OPC1 examine the virtual finishing time of all cells in the input queues and moves the cell with the lowest or smallest virtual finishing time across to the output queues (Step 1: Selection and request; Step 2: Grant; Step 3: Accept on left and right columns of pg 517). Cells become blocked from entering and moving to the switch when their virtual

finishing times are too large; and the cells are stored in the switch as they move across it.

With respect to claim 8, Chao discloses a Combined Input-Output Buffered (CIOB) switch using fixed-sized cells (Abstract, first paragraph, left column, pg 515) containing a multitude of input queues (session queues in IPC1 of Figure 3), a multitude of output queues (session queues in OPC1 of Figure 3); a switch fabric (X01, X11, X0, X1N of Figure 3; Non-blocking switch of Figure 1) that connects the multitude of input queues to the multitude of output queues and must have memory to store and move cells from the input queues to the output queues. Chao's CIOB switch also has an input port controller (IPC1 of Figure 3) and an output port controller (OPC1 of Figure 3) for calculating incoming cell priorities and moving cells from the input queues to the switch and moving cells from the switch to the output queues (Section V: The Implementation of the SHLS Scheme, right column, pg 519 – third paragraph, left column, pg 521).

In addition, the incoming cells are prioritizing based on the virtual time function of the output queue (Voj(t) in last paragraph, left column, pg 520).

Chao does not disclose a controller that determines input priorities for cells from input queues and output priorities for cells from switch fabric to output queues.

Wu, in a invention of scheduling cells across a switch crossbar (Abstract), discloses a controller (12 of Figure 2) that determines input priorities for cells from input queues and output priorities for cells from switch fabric to output queues (column 4, lines 14-26; column 5, lines 13-31).

Wu realizes the benefit of more scalability by using a dedicated controller to move cells/packets across the input queues, switch fabric, and output queues (column 2, lines 55-67). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the controller of Wu with the system of Chao.

With respect to claim 9, Chao further discloses that the cells with highest priority or minimum virtual finishing time are transferred by the IPC operations (last paragraph, right column, pg 519 --- first paragraph, left column, pg 520) and then the remaining cells are updated by a Xoj server during OAP(min) in the OAP operation phase (lines 1-3, left column, pg 521).

With respect to claim 12, Chao further discloses that output arbitration processor (OAP) and input arbitration processor (IAP) operations are performed by the switch (section V: The Implementation of the SHLS Scheme, first paragraph, right column, pg 519) where these operations are viewed as crosspoint schedulers.

With respect to claim 17, Chao discloses a method for a CIOB switch that moves fixed-sized cells (Abstract, first paragraph, left column, pg 515) contain the steps of select and moving cells with smallest virtual finishing timing (Step 3: Accept, left column, pg 517 – first paragraph, right column, pg 517) or higher priority from a fabric X01, X11, X0, X1N of Figure 3; Non-blocking switch of Figure 1) to output queues (session queues in OPC1 of Figure 3) where the cell is stored in the switch memory when it is moved;

updating priority information for cells by a Xoj server during OAP(min) in the OAP operation phase (lines 1-3, left column, pg 521);

selecting and moving cells with smallest virtual finishing timing (Step 3: Accept, left column, pg 517 – first paragraph, right column, pg 517) or higher priority from a input queues (session queues in IPC1 of Figure 3) to fabric X01, X11, X0, X1N of Figure 3; Non-blocking switch of Figure 1) based on update operation conducted during OAP(min); and

updating priority information (virtual times) for cells by a Xoj server during OAP(min) in the OAP operation phase (lines 1-3, left column, pg 521; first paragraph, right column, pg 522 where **"both packets use the new updated virtual time function to update their virtual starting time and virtual finishing time**").

Chao does not disclose a controller that determines input priorities for cells from input queues and output priorities for cells from switch fabric to output queues.

Wu, in a invention of scheduling cells across a switch crossbar (Abstract), discloses a controller (12 of Figure 2) that determines input priorities for cells from input queues and output priorities for cells from switch fabric to output queues (column 4, lines 14-26; column 5, lines 13-31).

Wu realizes the benefit of more scalability by using a dedicated controller to move cells/packets across the input queues, switch fabric, and output queues (column 2, lines 55-67). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the method of Wu with the method of Chao.

With respect to claim 18, Chao further discloses storing cells in the input queues according to their virtual finishing times or priorities (IPC operation, last paragraph, right column, pg 519) and the cells are moved through the switch memory

based on the output queue's virtual time function or its output priority (OAP operation, second paragraph, left column, pg 520).

With respect to claim 19, Chao further discloses that the steps for moving the cells across the switch are repeated for each cell in the queue, i.e. for each time slot in the queue (first paragraph, left column, pg 517 – last paragraph, right column, pg 517).

5. Claims 4, 5, 7, and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chao in view of Wu and further in view of Chuang et al. (Chuang et al., "Matching Output Queueing with a Combined Input/Output-Queued Switch", 30 June 1999, IEEE Journal on Selected Areas in Communications, Volume 17, pg 1030-1039; hereafter Chuang) cited in IDS dated 10/29/2003.

With respect to claim 4, Chao does not disclose the controllers determining an incoming cell's priority based on the time of the cell departing from an output queue and the times of other cells in the output queue to depart.

Chuang, in an invention of a cell-switching device, discloses a technique of inserting an incoming cell based on the number of cells in the output buffer with a smaller "time to leave" than the incoming cell (CCF Insertion Policy in second paragraph, left column, pg 1034).

Chuang realizes the advantage of less stall time for incoming cells that need to leave the switch faster due to Quality of Service demands. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use the technique of Chuang with the switch of Chao.

With respect to claim 5, Chao does not disclose the controller setting input and output priorities based on lowest time-to-leave scheduling, lowest time-to-leave blocking, and non-negative slackness insertion.

Chuang, in an invention of a cell-switching device, disclose a technique of input and output priority settings based on lowest time-to-leave scheduling (GBVOQ Algorithm, third paragraph, right column, pg 1035 where "**the cell which arrived earlier will have a smaller TL (Time-to-Leave) and hence a higher output priority**"), lowest time-to-leave blocking (GBVOQ Algorithm, third paragraph, right column, pg 1035 where "**to determine which of two cells has a higher output priority, we just need to compare the arrival timestamps of the two cells**"), and non-negative slackness insertion (CCF Insertion Policy in second and third paragraphs, left column, pg 1034).

Chuang realize the advantage of greater speedup values for packet switching with these scheduling techniques (the "OQ switch" advantage in third paragraph, right column, pg 1030). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use the technique of Chuang with the switch of Chao.

With respect to claim 7, Chao does not disclose the switch emulating an output queued packet switch.

Chuang, in an invention of a cell-switching device, disclose a technique to emulate an output queued packet switch by using lowest time-to-leave scheduling (GBVOQ Algorithm, third paragraph, right column, pg 1035 where "**the cell which arrived earlier will have a smaller TL (Time-to-Leave) and hence a higher output priority**"), lowest time-to-leave blocking (GBVOQ Algorithm, third paragraph, right

column, pg 1035 where "**to determine which of two cells has a higher output priority, we just need to compare the arrival timestamps of the two cells**"), and non-negative slackness insertion (CCF Insertion Policy in second and third paragraphs, left column, pg 1034).

Chuang realize the advantage of greater speedup values for packet switching with these scheduling techniques (the "OQ switch" advantage in third paragraph, right column, pg 1030). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use the technique of Chuang with the switch of Chao.

With respect to claim 10, Chao does not disclose the controllers determining an incoming cell's priority based on the time of the cell departing from an output queue and the times of other cells in the output queue to depart.

Chuang, in an invention of a cell switching device, discloses a technique of inserting an incoming cell based on the number of cells in the output buffer with a smaller "time to leave" than the incoming cell (CCF Insertion Policy in second paragraph, left column, pg 1034).

Chuang realizes the advantage of less stall time for incoming cells that need to leave the switch faster due to Quality of Service demands. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use the technique of Chuang with the switch of Chao.

6. Claims 6, 11, 13, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chao in view of Wu and further in view of Rojas-Cessa et al. (Rojas-Cessa et al., "CIXB-1: Combined Input-One-cell-Crosspoint Buffered Switch", 31 May

2001, 2001 IEEE Workshop on High Performance Switching and Routing, pg 324-329; hereafter Rojas-Cessa) cited in IDS dated 10/29/2003.

With respect to claim 6, Chao fails to disclose a switch that is a buffered crossbar switch fabric.

Rojas-Cessa, in a related switch invention, discloses a switch with crosspoint buffers (XPB of Figure 1).

Rojas-Cessa teaches the advantage of increased throughtput by using buffers in the switch (fourth paragraph, right column, pg 325). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use the switch structure of Rojas-Cessa with the switch of Chao.

With respect to claim 11, Chao discloses a multitude of input schedulers and a fabric scheduler (section V: The Implementation of the SHLS Scheme, first paragraph, right column, pg 519) where these operations are viewed as the fabric scheduler.

Chao fails to disclose a flow control mechanism with the switch.

Rojas-Cessa, in a related switch invention, discloses a flow control mechanism (last paragraph, left column, pg 326; "**Flow Control. A flow control mechanism tells the input port i...**") as part of a crossbar switch.

Rojas-Cessa teaches the advantage of increased throughtput by using buffers in the switch and a flow control mechanism (fourth paragraph, right column, pg 325). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use the switch structure of Rojas-Cessa with the switch of Chao.

With respect to claim 13, Chao fails to disclose that the input queues are build from several virtual output queues.

Rojas-Cessa, in a related switch invention, discloses a switch with virtual output queues (VOQs) at the input ports (Input 0, Input N-1 of Figure 1; fifth paragraph, left column, pg 326, second bullet states "**Input Queue: There are VOQs at the input ports. A VOQ at input I that stores cells for output j is denoted VOQi,j**").

Rojas-Cessa teaches the advantage of increased throughtput by using VOQs in the switch (second paragraph, right column, pg 324). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use the switch structure of Rojas-Cessa with the switch of Chao.

With respect to claim 14, Chao fails to disclose a switch containing multiple crosspoint buffers and having the crosspoint buffers connects to virtual output queues (VOQs).

Rojas-Cessa, in a related switch invention, discloses a switch with virtual output queues (VOQs) at the input ports (Input 0, Input N-1 of Figure 1; fifth paragraph, left column, pg 326, second bullet states "**Input Queue: There are VOQs at the input ports. A VOQ at input I that stores cells for output j is denoted VOQi,j**") and connected crosspoint buffers (XPB of Figure 1).

Rojas-Cessa teaches the advantage of increased throughtput by using VOQs in the switch (second paragraph, right column, pg 324) and crosspoint buffers (fourth paragraph, right column, pg 325). Thus it would have been obvious to one of ordinary

skill in the art at the time of the invention to use the switch structure of Rojas-Cessa with the switch of Chao.

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chao in view of Wu and further in view of Zhang (Zhang, "Service Disciplines for Guaranteed Performance Service in Packet-Switching Networks", 31 October 1995, Proceedings of the IEEE, pg 1374-1396).

With respect to claim 15, Chao fails to disclose input queues that contain first-in-first-out (FIFO) groups.

Zhang, in a related field of endeavor, teaches FIFOs groups sharing a single link (Section B: WFQ and WF2Q, first paragraph, right column, pg 1378; "**these is a separate FIFO queue for each connection sharing the same link**").

Zhang realizes the advantage of increases quality of service offers by group the FIFOs in a single link (Section B: WFQ and WF2Q, first paragraph, right column, pg 1378; "**FFQ allows different connections to have different service shares**"). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use the technique of Zhang with the switch of Chao.

8. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chao in view of Wu and further in view of Rojas-Cessa and further in view of Zhang.

With respect to claim 16, Chao fails to disclose a switch containing multiple crosspoint buffers.

Rojas-Cessa, in a related switch invention, discloses a switch with crosspoint buffers (XPB of Figure 1).

Rojas-Cessa teaches the advantage of increased throughtput by using crosspoint buffers (fourth paragraph, right column, pg 325). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use the switch structure of Rojas-Cessa with the switch of Chao.

Chao fails to disclose input queues that contain first-in-first-out (FIFO) groups.

Zhang, in a related field of endeavor, teaches FIFOs groups sharing a single link (Section B: WFQ and WF2Q, first paragraph, right column, pg 1378; "**these is a separate FIFO queue for each connection sharing the same link**").

Zhang realizes the advantage of increases quality of service offers by group the FIFOs in a single link (Section B: WFQ and WF2Q, first paragraph, right column, pg 1378; "**FFQ allows different connections to have different service shares**"). Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use the technique of Zhang with the switch of Chao and Rojas-Cessa.

Response to Arguments

9. Applicant's arguments filed on 03/27/2008 have been fully considered but they are not persuasive.

A) Applicant argues, with respect to claim 1, that Chao does not represent an exemplary switch architecture.

The Examiner maintains the rejection over Chao in view of Wu because Chao clearly discloses a switching architecture in Figure 3 on page 519. Input signals are moved to output ports through processing switches.

B) Applicant argues, with respect to claim 1, that Wu does not disclose a controller determining input priorities for cells.

The Examiner maintains the rejection over Chao in view of Wu because Wu's system operates on a number of different channels (STS-1-Xv, STS-3c-Sv, STS-12c, STS-24c) and mixed these channels with a given priority for each channel.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRIAN T. O'CONNOR whose telephone number is (571)270-1081. The examiner can normally be reached on 9:00AM-6:30PM, M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571-272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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July 3, 2007
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